

Appl. No. 09/931,088  
Customer No. 27683

**Listing of Claims:**

1-18. (canceled).

19. (currently amended) A network processing device, comprising:

an ingress circuit configured to process packets received over a network;

an egress circuit configured to process packets for sending over the network;

a reconfigurable switch fabric for transferring packets scrambled data between a plurality of switch fabric ports between the ingress circuit and the egress circuit; and

a first scrambler circuit configured to scramble a first parallel array of packet bits received from the ingress circuit into [[an]] a first array of scrambled output bits during a same current clock period for switching across the switch fabric towards the egress circuit.

20. (currently amended) A network processing device according to claim 19 including a first new seed register for storing [[an]] the first array of scrambled output bits from a previous clock period and supplying the first array of scrambled output bits to the first scrambler circuit for applying to [[the]] a second parallel array of bits received from the ingress circuit from the packet data.

21. (currently amended) A network processing device according to claim 20, further comprising including a first scrambler circuit and new seed register located in the ingress circuit for scrambling the array of packet bits before being transferred over the switch fabric and a second scrambler circuit and a second new seed register located in the egress circuit for scrambling the packets processed by the egress circuit array of packet bits before being transferred sending those packets over the network.

22. (currently amended) A network processing device according to claim 20, further comprising including a first de-scrambler circuit coupled to the egress circuit and configured to receive scrambled data from the switch fabric, the scrambled data comprising the first array of scrambled output bits, and de-scramble the first array of scrambled output packet bits into [[an]] a first array of descrambled packet bits during a same current clock period.

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23. (currently amended) A network processing device according to claim 22 including a first de-scrambler new seed register for storing ~~[[an]]~~ the first array of de-scrambled packet bits ~~from a previous clock period~~ and supplying the first array of de-scrambled output bits to the first de-scrambler circuit for applying to a second array of scrambled output bits received from the switch fabric ~~the scrambled packet bits during the current clock period.~~

24. (currently amended) A network processing device according to claim 23, further comprising ~~including a first~~ a second de-scrambler circuit and a second de-scrambler new seed register located in the ingress circuit for descrambling arrays of scrambled bits ~~after being received from the network and a second descrambler circuit and new seed register located in the egress circuit for de-scrambling arrays of scrambled output bits received over the switch fabric.~~

25. (new) A method for switching packet data between a plurality of network ports, comprising:  
receiving packet data from a network;  
scrambling a first parallel array of bits from the packet data into an array of first scrambled output bits;  
transferring the first scrambled output bits through a reconfigurable switch fabric; and  
descrambling the first scrambled output bits after transferring the first scrambled output bits through the reconfigurable switch fabric.

26. (new) A method according to claim 25 including storing the first scrambled output bits as new seed values for applying scramble polynomials to a second parallel array of bits from the packet data.

27. (new) A method according to claim 26 including selecting the new seed values according to scramble polynomial values, a bit length of the parallel arrays of bits, and a position of the individual bits in the parallel arrays of input bits.

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28. (new) A method according to claim 26 including using the stored first scrambled output bits to apply a  $1 + X(39) + X(58)$  scramble polynomial to each one of the second parallel array of input bits.

29. (new) A method according to claim 25 wherein descrambling the first scrambled output bits comprises:

receiving the first scrambled output bits;

storing an array of previously de-scrambled output bits; and

applying the array of previously de-scrambled output bits during descrambling of the first scrambled output bits.

30. (new) A method according to claim 29 including storing the first de-scrambled output bits as new seed values for applying to a next group of scrambled output bits.